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| 10/809,749 | 03/25/2004 | Brian Robert Prasky | POU920030065US1 | 7321 |

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| EXAMINER | |
|---|---|
| FENNEMA, ROBERT E | |
| ART UNIT | PAPER NUMBER |
| 2183 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/809,749 | PRASKY ET AL. | |
| | Examiner | Art Unit | |
| | Robert E. Fennema | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-30 are pending.

### *Claim Objections*

2. Claims 2-10, 12-20, and 22-30 are objected to for referring to "A" (method/system/product), instead of "The", and it is unclear if the claims are referring to a different (method/system/product) than the claims upon which they depend, or the same ones.

3. Claims 6-7, 16-17, and 26-27 are objected to for referring to the "instruction field", when no instruction field has been introduced. It has been assumed that this should read the "instruction text field", and has been interpreted as such for the remainder of this Office Action.

4. Claims 6, 16, and 26 are objected to for the recitation of "... into the BTB in system ...". It is unclear what this statement means. Further, it is unclear what is meant by "whereby the branch is blocked", which could be interpreted as blocked from entering the BTB, or blocked from executing entirely. It has been interpreted to be the former, in accordance with the language of the independent claims for the remainder of the Office Action.

5. Claims 9, 19, and 29 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 9, 19, and 29 do not further limit their patent claim, as they simply suggest an intended use for the bit to prevent the branch being placed into the BTB. See MPEP 2106 [R-3] II.C, which states that claims which use language which suggests or makes optional does not limit the scope of the claim.

6. Claims 1-30 are objected to for the use of the word "define". It is not clear what exactly the applicant is claiming by "defining", whether it be setting a bit, determining the value of a bit, or determining which bit in a string of bits is something to look at. Applicant is requested to clarify the scope of "define", or to use language that helps to more clearly identify what the Applicant is claiming as the invention. Examiner has interpreted "define" for this Office Action to be some indication in a bit of an instruction that allows the functionality of the claims.

### *Claim Rejections - 35 USC § 101*

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1-30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims in question are associated with

what appears to be just a determining step of "defining a bit", yet producing no tangible result, as nothing appears to be done as a result of this definition. Instead, Claims 1, 11, and 21 refer to an intended use of the definition of the bit, but does not state that this action is undertaken, thus making the Claim non-statutory. Claims 2-10, 12-20, and 22-30 fail to correct the deficiencies of the Claim and are rejected for the same reasons.

### *Claim Rejections - 35 USC § 103*

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Check et al. (USPN 6,125,444, herein Check), in view of Patterson et al. (herein Patterson).

11. As per Claim 1, Check teaches: A method operating a computer having a pipelined processor (Figure 1), comprising defining a bit within an instruction text field of a branch (Column 2, Lines 33-40 and Column 4, Lines 24-27), but fails to teach:

whereby to prevent the branch from being placed into a branch target buffer to thereby make the branch only detectable as the time frame of decode.

While Check teaches using an instruction field of an instruction to disable a branch history table, he does not teach that doing so would prevent the branch from

being placed in a branch target buffer. However, Patterson teaches that in order to further increase the performance of branches, a "branch target buffer" is often used, so that the target address can be calculated in the fetch stage, instead of the decode stage (Pages 271-275). As the branch target buffer relies on having a prediction in order to determine the correct address, as seen by Figure 4.23 on Page 275, if no prediction was able to be generated, because of a BHT being disabled, then it would have been obvious to one of ordinary skill in the art to also not use the BTB, as it would not have the data it needs to be made use of. In addition, as can be seen by Column 2, Lines 28-31, sensitive system operations require cache control, so for the same reason Check disables the BHT, the BTB would need to not be written to as well. Given the advantage of a BTB as disclosed by Patterson, and the need to implement it in the system as disclosed by Check, one of ordinary skill in the art at the time the invention was made would have been motivated to include a BTB, and also to disable its use when the BHT was disabled.

12. As per Claim 2, Check teaches: A method as defined in claim 1 comprising predicting the direction and target of a branch prior to decode (Figure 1).

13. As per Claim 3, Check teaches: A method as defined in claim 2 comprising predicting the direction and target of a branch prior to decode through a branch prediction array (Figure 1, also see Column 4, Lines 32-49).

14. As per Claim 4, Check teaches: A method as defined in claim 1 comprising tracking the branch from the beginning of the pipe, decode, until the time frame that the given instruction is to be written into a branch prediction array (It is inherent that instructions in a pipeline are kept track of, they must exist until they are removed).

15. As per Claim 5, Check teaches: A method as defined in claim 1 comprising denoting the instruction text field as a non-writable branch into the BTB (Column 2, Lines 36-40).

16. As per Claim 6, Check teaches: A method as defined in claim 5 denoting the instruction field in the system area as a non-writable branch into the BTB in system whereby the branch is blocked (Column 2, Lines 28-31).

17. As per Claim 7, Check teaches: A method as defined in claim 5 denoting the instruction field in the non-system area, the branch may be predicted via aliasing (Column 4, Lines 12-15).

18. As per Claim 8, Patterson teaches: A method as defined in claim 1 wherein machine state altering code lies within an address range spanned by branch tag bits of the branch target buffer (All instructions can alter machine state, so if any instruction is in the BTB, machine state altering code lies within an address range spanning by tag

bits in the BTB).

19. As per Claim 9, Check teaches: A method defined in claim 4 where branches which have targets that are highly non-constant can be blocked from branch predictions through the use the BTB blocking field in the instruction text (Column 2, Lines 50-59).

20. As per Claim 10, Check teaches: The method as defined in claim 8 comprising denoting state altering code in the system area by a state bit within the BTB/BHT such that aliasing of branches is prevented within the system area (Column 2, Lines 28-40).

21. As per Claim 11, Check teaches: A computer system having input, output, storage, and a pipelined processor (Figure 1), said processor adapted and configured to define a bit within an instruction text field of a branch (Column 2, Lines 33-40 and Column 4, Lines 24-27), but fails to teach: whereby to prevent the branch from being placed into a branch target buffer to thereby make the branch only detectable as the time frame of decode.

While Check teaches using an instruction field of an instruction to disable a branch history table, he does not teach that doing so would prevent the branch from being placed in a branch target buffer. However, Patterson teaches that in order to further increase the performance of branches, a "branch target buffer" is often used, so that the target address can be calculated in the fetch stage, instead of the decode stage (Pages 271-275). As the branch target buffer relies on having a prediction in order to

determine the correct address, as seen by Figure 4.23 on Page 275, if no prediction was able to be generated, because of a BHT being disabled, then it would have been obvious to one of ordinary skill in the art to also not use the BTB, as it would not have the data it needs to be made use of. In addition, as can be seen by Column 2, Lines 28-31, sensitive system operations require cache control, so for the same reason Check disables the BHT, the BTB would need to not be written to as well. Given the advantage of a BTB as disclosed by Patterson, and the need to implement it in the system as disclosed by Check, one of ordinary skill in the art at the time the invention was made would have been motivated to include a BTB, and also to disable its use when the BHT was disabled.

22. As per Claim 12, Check teaches: A computer system as defined in claim 11, said computer system adapted and configured to predict the direction and target of a branch prior to decode (Figure 1).

23. As per Claim 13, Check teaches: A computer system as defined in claim 12 said computer system adapted and configured to predict the direction and target of a branch prior to decode through a branch prediction array (Figure 1, also see Column 4, Lines 32-49).

24. As per Claim 14, Check teaches: A computer system as defined in claim 11, said computer system adapted and configured to track the branch from the beginning of the

pipe, decode, until the time frame that the given instruction is to be written into a branch prediction array (It is inherent that instructions in a pipeline are kept track of, they must exist until they are removed).

25. As per Claim 15, Check teaches: A computer system as defined in claim 11 said computer system adapted and configured to denote the instruction text field as a non-writable branch into the BTB (Column 2, Lines 36-40).

26. As per Claim 16, Check teaches: A computer system as defined in claim 15 said computer system adapted and configured to denote the instruction field in the system area as a non-writable branch into the BTB in system whereby the branch is blocked (Column 2, Lines 28-31).

27. As per Claim 17, Check teaches: A computer system as defined in claim 15 said computer system adapted and configured to denote the instruction field in the non-system area, the branch may be predicted via aliasing (Column 4, Lines 12-15).

28. As per Claim 18, Patterson teaches: A computer system as defined in claim 11 wherein machine state altering code lies within an address range spanned by branch tag bits of the branch target buffer (All instructions can alter machine state, so if any instruction is in the BTB, machine state altering code lies within an address range

spanning by tag bits in the BTB).

29. As per Claim 19, Check teaches: A computer system as defined in claim 14 where branches which have targets that are highly non-constant can be blocked from branch predictions through the use the BTB blocking field in the instruction text (Column 2, Lines 50-59).

30. As per Claim 20, Check teaches: A computer system as defined in claim 18 said computer system is adapted and configured to denote state altering code in the system area by a state bit within the BTB/BHT such that aliasing of branches is prevented within the system area is prevented (Column 2, Lines 28-40).

31. As per Claim 21, Check teaches: A program product comprising a storage medium having computer readable program code, said program code for use in a computer system having input, output, storage, and a pipelined processor (Figure 1), said program code adapting and configuring the computer system to define a bit within an instruction text field of a branch (Column 2, Lines 33-40 and Column 4, Lines 24-27), but fails to teach:

whereby to prevent the branch from being placed into a branch target buffer to thereby make the branch only detectable as the time frame of decode.

While Check teaches using an instruction field of an instruction to disable a branch history table, he does not teach that doing so would prevent the branch from

being placed in a branch target buffer. However, Patterson teaches that in order to further increase the performance of branches, a "branch target buffer" is often used, so that the target address can be calculated in the fetch stage, instead of the decode stage (Pages 271-275). As the branch target buffer relies on having a prediction in order to determine the correct address, as seen by Figure 4.23 on Page 275, if no prediction was able to be generated, because of a BHT being disabled, then it would have been obvious to one of ordinary skill in the art to also not use the BTB, as it would not have the data it needs to be made use of. In addition, as can be seen by Column 2, Lines 28-31, sensitive system operations require cache control, so for the same reason Check disables the BHT, the BTB would need to not be written to as well. Given the advantage of a BTB as disclosed by Patterson, and the need to implement it in the system as disclosed by Check, one of ordinary skill in the art at the time the invention was made would have been motivated to include a BTB, and also to disable its use when the BHT was disabled.

32. As per Claim 22, Check teaches: A program product as defined in claim 21, said computer system adapted and configured to predict the direction and target of a branch prior to decode (Figure 1).

33. As per Claim 23, Check teaches: A program product as defined in claim 22 said computer system adapted and configured to predict the direction and target of a branch prior to decode through a branch prediction array (Figure 1, also see Column 4, Lines

32-49).

34. As per Claim 24, Check teaches: A program product as defined in claim 21, said computer system adapted and configured to track the branch from the beginning of the pipe, decode, until the time frame that the given instruction is to be written into a branch prediction array (It is inherent that instructions in a pipeline are kept track of, they must exist until they are removed).

35. As per Claim 25, Check teaches: A program product as defined in claim 21 said computer system adapted and configured to denote the instruction text field as a non-writable branch into the BTB (Column 2, Lines 36-40).

36. As per Claim 26, Check teaches: A program product as defined in claim 25 said computer system adapted and configured to denote the instruction field in the system area as a non-writable branch into the BTB in system whereby the branch is blocked (Column 2, Lines 28-31).

37. As per Claim 27, Check teaches: A program product as defined in claim 25 said computer system adapted and configured to denote the instruction field in the non-system area, the branch may be predicted via aliasing (Column 4, Lines 12-15).

38. As per Claim 28, Patterson teaches: A program product as defined in claim 21 wherein machine state altering code lies within an address range spanned by branch tag bits of the branch target buffer (All instructions can alter machine state, so if any instruction is in the BTB, machine state altering code lies within an address range spanning by tag bits in the BTB).

39. As per Claim 29, Check teaches: A program product as defined in claim 24 where branches which have targets that are highly non-constant can be blocked from branch predictions through the use the BTB blocking field in the instruction text (Column 2, Lines 50-59).

40. As per Claim 30, Check teaches: A program product as defined in claim 28 said computer system is adapted and configured to denote state altering code in the system area by a state bit within the BTB/BHT such that aliasing of branches is prevented within the system area (Column 2, Lines 28-40).

***Conclusion***

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must

also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

42. Ishimoto et al. (USPN 6,101,586) teaches a method to block branches going to protected areas of memory.

43. Check et al. (USPN 6,108,776) teaches a register to disable or enable the branch history table.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema
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